CLAIMS

What is claimed is:

1. A method of operating a synchronous circuit, comprising:
obtaining a reference clock and an inverted reference clock for said synchronous circuit;
using a delay line as part of said synchronous circuit to generate a feedback clock; and
selectively using one of said reference clock and said inverted reference clock as an input to said delay line based on a relationship among the phases of said reference clock, said inverted reference clock, and said feedback clock.

2. The method of claim 1, further comprising obtaining a delayed feedback clock by delaying said feedback clock by a predetermined time delay.

3. The method of claim 2, wherein said selectively using includes:
sampling said reference clock and said inverted reference clock using said feedback clock to obtain a first logic value and a second logic value respectively;
further sampling said reference clock and said inverted reference clock using said delayed feedback clock to obtain a third logic value and a fourth logic value respectively; and
using said inverted reference clock as said input to said delay line so long as said fourth logic value is "0" and said third logic value is "1" along with a value of "1" for one of said first and said second logic values.

4. The method of claim 2, further comprising:
using said delayed feedback clock to determine said relationship among the phases of said reference clock, said inverted reference clock, and said feedback clock.

5. The method of claim 4, wherein said selectively using includes:
sampling said reference clock and said inverted reference clock using said delayed feedback clock to obtain a first logic value and a second logic value respectively; and
using said inverted reference clock as said input to said delay line so long as said first

logic value is "1" and said second logic value is "0".

6. A method of operating a synchronous circuit, comprising:
obtaining a reference clock and an inverted reference clock for said synchronous circuit;
using a delay line as part of said synchronous circuit to generate a feedback clock;
obtaining a delayed feedback clock from said feedback clock; and
selectively using one of said reference clock and said inverted reference clock as an input to said delay line based on a relationship among the phases of said reference clock, said inverted reference clock, said feedback clock and said delayed feedback clock.

7. The method of claim 6, wherein obtaining said delayed feedback clock includes delaying said feedback clock by a predetermined time delay to obtain said delayed feedback clock.

8. The method of claim 7, further comprising adjusting said predetermined time delay based on at least one of the following:
how far away a lock point of said synchronous circuit establishing a lock between said reference clock and said feedback clock can be moved from an initial entry point;
frequency of said feedback clock; and
a tuning range of said synchronous circuit after establishing said lock between said reference clock and said feedback clock.

9. The method of claim 6, wherein said selectively using includes:
obtaining a first phase relationship between said feedback clock and said reference clock;
obtaining a second phase relationship between said feedback clock and said inverted reference clock;
obtaining a third phase relationship between said delayed feedback clock and said reference clock;
obtaining a fourth phase relationship between said delayed feedback clock and said inverted reference clock; and
using said inverted reference clock as said input to said delay line based on said first, said

second, said third, and said fourth phase relationships.

10. The method of claim 9, wherein using said inverted reference clock as said input includes using said inverted reference clock as said input so long as said fourth phase relationship has a logic value of "0" and said third phase relationship has a logic value of "1" along with a logic value of "1" for one of said first and said second phase relationships.

11. The method of claim 9, wherein said first phase relationship is a first logic value obtained when said reference clock is sampled by said feedback clock, wherein said second phase relationship is a second logic value obtained when said inverted reference clock is sampled by said feedback clock, wherein said third phase relationship is a third logic value obtained when said reference clock is sampled by said delayed feedback clock, and said fourth phase relationship is a fourth logic value obtained when said inverted reference clock is sampled by said delayed feedback clock, and wherein using said inverted reference clock as said input includes:

using said inverted reference clock as said input so long as said fourth logic value is "0" and said third logic value is "1" along with a value of "1" for one of said first and said second logic values.

12. The method of claim 6, wherein said selectively using includes:

sampling said reference clock and said inverted reference clock using said feedback clock to obtain a first logic value and a second logic value respectively;

further sampling said reference clock and said inverted reference clock using said delayed feedback clock to obtain a third logic value and a fourth logic value respectively; and

using said inverted reference clock as said input to said delay line so long as said fourth logic value is "0" and said third logic value is "1" along with a value of "1" for one of said first and said second logic values.

13. The method of claim 6, wherein said selectively using includes:

sampling said reference clock and said inverted reference clock using said delayed

feedback clock to obtain a first logic value and a second logic value respectively; and

using said inverted reference clock as said input to said delay line so long as said first logic value is "1" and said second logic value is "0".

14. A method of operating a synchronous circuit, comprising:

obtaining a reference clock and an inverted reference clock for said synchronous circuit;

using a delay line as part of said synchronous circuit to generate a feedback clock;

obtaining a delayed feedback clock from said feedback clock; and

selectively using one of said reference clock and said inverted reference clock as an input to said delay line based on individual sampling of said reference clock and said inverted reference clock with each of said feedback clock and said delayed feedback clock.

15. The method of claim 14, wherein said individual sampling is performed to establish a relationship among the phases of said reference clock, said inverted reference clock, said feedback clock and said delayed feedback clock.

16. The method of claim 14, wherein obtaining said delayed feedback clock includes delaying said feedback clock by a predetermined time delay to obtain said delayed feedback clock.

17. The method of claim 14, wherein said selectively using includes:

obtaining a first sample of said reference clock using said feedback clock;

obtaining a second sample of said inverted reference clock using said feedback clock;

obtaining a third sample of said reference clock using said delayed feedback clock;

obtaining a fourth sample of said inverted reference clock using said delayed feedback clock; and

using said inverted reference clock as said input to said delay line based on logic values of said first, said second, said third, and said fourth samples.

18. The method of claim 17, wherein using said inverted reference clock as said input includes:

using said inverted reference clock as said input so long as said fourth sample has logic value of "0" and said third sample has logic value of "1" along with a logic value of "1" for one of said first and said second samples.

19. A synchronous circuit, comprising:

a delay line to receive an input clock and to generate a feedback clock therefrom, wherein said delay line is configured to provide a predetermined delay to said input clock to generate said feedback clock therefrom; and

a decoder circuit coupled to said delay line and configured to receive said feedback clock as a first input and to generate a delayed feedback clock therefrom, wherein said decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, wherein said decoder circuit is configured to determine a relationship among the phases of said reference clock, said inverted reference clock, said feedback clock, and said delayed feedback clock, and to selectively supply one of said reference clock and said inverted reference clock as said input clock to said delay line based on determination of said phase relationship.

20. The circuit of claim 19, further comprising:

a phase detector coupled to said delay line and configured to receive said reference clock and said feedback clock as inputs thereto, wherein said phase detector is configured to determine a phase relationship between said feedback clock and said reference clock and to responsively provide a delay adjustment indication to said delay line so as to enable said delay line to delay said input clock based on said delay adjustment indication.

21. The circuit of claim 19, wherein said decoder circuit is configured to generate a switching signal based on said relationship among the phases of said reference clock, said inverted reference clock, said feedback clock, and said delayed feedback clock.

22. The circuit of claim 21, wherein said decoder circuit is configured to supply said inverted reference clock as said input clock to said delay line when said switching signal is in an active state.

23. The circuit of claim 22, wherein said active state is active high.

24. The circuit of claim 21, wherein said decoder circuit includes:

a delay element to receive said feedback clock as input thereto and to generate said delayed feedback clock as output thereof;

a first sampler circuit configured to receive said reference clock, said inverted reference clock and said feedback clock as inputs thereto and to responsively generate a first indication signal and a second indication signal therefrom;

a second sampler circuit configured to receive as inputs thereto said reference clock, said inverted reference clock and said delayed feedback clock from said delay element and to responsively generate a third indication signal and a fourth indication signal therefrom; and

a switch signal generator configured to receive said first, said second, said third, and said fourth indication signals, and to generate said switching signal therefrom.

25. The circuit of claim 24, wherein said first indication signal is obtained when said reference clock is sampled by said feedback clock, wherein said second indication signal is obtained when said inverted reference clock is sampled by said feedback clock, wherein said third indication signal is obtained when said reference clock is sampled by said delayed feedback clock, and said fourth indication signal is obtained when said inverted reference clock is sampled by said delayed feedback clock, and wherein said switch signal generator is configured to generate said switching signal when all of the following apply:

said fourth indication signal has a logic "0" value;

said third indication signal has a logic "1" value; and

one of said first and said second indication signals has a logic "1" value.

26. The circuit of claim 21, wherein said decoder circuit includes:

a delay element to receive said feedback clock as input thereto and to generate said delayed feedback clock as output thereof;

a sampler circuit configured to receive as inputs thereto said reference clock, said inverted reference clock and said delayed feedback clock from said delay element and to responsively generate a first indication signal and a second indication signal therefrom; and

a switch signal generator configured to receive said first and said second indication signals, and to generate said switching signal therefrom.

27. The circuit of claim 26, wherein said first indication signal is obtained when said reference clock is sampled by said delayed feedback clock, and said second indication signal is obtained when said inverted reference clock is sampled by said delayed feedback clock, and wherein said switch signal generator is configured to generate said switching signal when both of the following apply:

said first indication signal has a logic "1" value; and

said second indication signal has a logic "0" value.

28. A combination, comprising:

a plurality of memory cells to store data;

a memory controller in communication with said plurality of memory cells to facilitate a data write/read operation at one of said plurality of memory cells; and

a delay locked loop configured to provide a feedback clock during reading of data as part of said data write/read operation, wherein said delay locked loop includes:

a delay line to receive an input clock and to generate a feedback clock therefrom, wherein said delay line is configured to provide a predetermined delay to said input clock to generate said feedback clock therefrom, and

a decoder circuit coupled to said delay line and configured to receive said feedback clock as a first input and to generate a delayed feedback clock therefrom, wherein said decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third

input, wherein said decoder circuit is configured to determine a relationship among the phases of said reference clock, said inverted reference clock, and at least one of said feedback clock and said delayed feedback clock, and to selectively supply one of said reference clock and said inverted reference clock as said input clock to said delay line based on determination of said phase relationship.

29. A synchronous circuit, comprising:

a delay line to receive an input clock and to generate a feedback clock therefrom, wherein said delay line is configured to provide a predetermined delay to said input clock to generate said feedback clock therefrom; and

a decoder circuit coupled to said delay line and configured to receive said feedback clock as a first input and to generate a delayed feedback clock therefrom, wherein said decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, wherein said decoder circuit is configured to determine a relationship among the phases of said reference clock, said inverted reference clock, and said delayed feedback clock, and to selectively supply one of said reference clock and said inverted reference clock as said input clock to said delay line based on determination of said phase relationship.

30. A system, comprising:

a processor;

a bus; and

a memory device coupled to said processor via said bus, wherein said memory device includes:

a synchronous circuit having:

a delay line to receive an input clock and to generate a feedback clock therefrom, wherein said delay line is configured to provide a predetermined delay to said input clock to generate said feedback clock therefrom, and

a decoder circuit coupled to said delay line and configured to receive said

feedback clock as a first input and to generate a delayed feedback clock therefrom, wherein said decoder circuit is further configured to receive a reference clock as a second input and an inverted reference clock as a third input, wherein said decoder circuit is configured to determine a relationship among the phases of said reference clock, said inverted reference clock, and at least one of said feedback clock and said delayed feedback clock, and to selectively supply one of said reference clock and said inverted reference clock as said input clock to said delay line based on determination of said phase relationship.

31. A method of operating a synchronous circuit, comprising:
obtaining a reference clock and an inverted reference clock for said synchronous circuit;
using a delay line as part of said synchronous circuit to generate a feedback clock;
obtaining a delayed feedback clock from said feedback clock; and
selectively using one of said reference clock and said inverted reference clock as an input to said delay line based on individual sampling of said reference clock and said inverted reference clock with said delayed feedback clock.

32. The method of claim 31, wherein said individual sampling is performed to establish a relationship among the phases of said reference clock, said inverted reference clock, and said delayed feedback clock.

33. The method of claim 31, wherein obtaining said delayed feedback clock includes delaying said feedback clock by a predetermined time delay to obtain said delayed feedback clock.

34. The method of claim 31, wherein said selectively using includes:
obtaining a first sample of said reference clock using said delayed feedback clock;
obtaining a second sample of said inverted reference clock using said delayed feedback clock; and

using said inverted reference clock as said input to said delay line based on logic values of said first, and said second samples.

35. The method of claim 34, wherein using said inverted reference clock as said input includes:

using said inverted reference clock as said input so long as said first sample has logic value of "1" and said second sample has logic value of "0".

36. A method of operating a synchronous circuit, comprising:

obtaining a reference clock and an inverted reference clock for said synchronous circuit;

using a delay line as part of said synchronous circuit to generate a feedback clock;

obtaining a delayed feedback clock from said feedback clock; and

selectively using one of said reference clock and said inverted reference clock as an input to said delay line based on a relationship among the phases of said reference clock, said inverted reference clock, and one of said feedback clock and said delayed feedback clock.